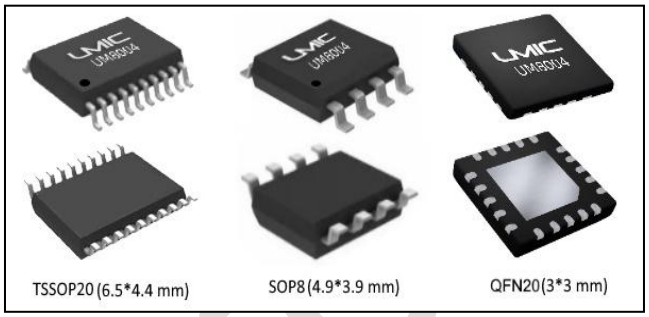
UNICMICRO 广芯微电子

UM8004

Ultra-low Power 8-bit MCU: 1T8051, 16KB eFlash, 2 KB + 256 B SRAM, 12-bit ADC, No Crystal/LDO/RC Circuit, Rich Interfaces, Anti-crash, Anti-copy

Product Features

- **Ultra-low power management system**
  - 1.1 µA @ 3.0 V DeepSleep mode + timed wakeup, running at low clock speed, data retention for IO, SRAM and register
  - 0.75 µA @ 3.0 V Stop mode, clock source stop, data retention for IO, SRAM and register
  - 80 µA/MHz @ 3.0 V Active mode
  - Built-in ROSC/LDO/POR, board-level system requires no crystal/LDO/reset circuit
- **Core**
  - 8-bit high-performance 8051 MCU, 1T, 6–12 times faster than the regular 8051
- **Memory**
  - RAM: 256 B Idata, 1 KB Xdata
  - 16 KB eFlash / 1 KB EEPROM
- **GPIO:** up to 17 pcs, configurable pull up/down
- **Timer/counter**
  - 2 × 16-bit GTimers supporting complementary PWM output with dead-time insertion
  - 1 x 16-bit LPTimer with PWM output
  - 1 x Watchdog timer WDT
- **Clock**
  - Internal RCH: 24 MHz
  - Internal RCL: 38 kHz
  - External crystal oscillator: 24 MHz (max.)
  - External clock input: 24 MHz (max.)
- **Communication interface**
  - PWM: 9 × 16-bit PWM outputs
  - UART: UART0 / UART1 / UART2 / UART3
  - I2C: master/slave, up to 400 kbps
  - SPI: 1 channel, master/slave, Mode 0/1/2/3 protocol, up to 12 Mbps



- **Analog peripherals**
  - ADC: 8-channel 12-bit SAR ADC, 1 Msps sampling rate
  - BEEPER: buzzer, configurable output frequency / polarity
  - Low-voltage detection (LVD), monitoring supply voltage
  - Low-voltage reset (LVR), anti-crash
  - Hardware-level anti-copy board
  - 16-byte UUID
- **Electrical Characteristics**
  - Operating voltage: 2.5 V–5.5 V
  - Operating temperature:
    -40℃ ~ 105℃ (≤16 MHz)
    -40℃ ~ 85℃ (24 MHz)
  - ESD: 8 kV (HBM)
- **Development support**
  - Bootloader, supporting download via UART & updating of ISP and IAP programs
  - Complete SDK and EVB HDK
  - Offline programmer and UMP tool
- **Order selection**

Model	Type
16 KB	UM8004-ACTE (TSSOP20) UM8004-ACSA (SOP8) UM8004-ACQE (QFN20)

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1 Overview

UM8004 is a low-power 8-bit IoTP processor developed by Unicmicro based on single-cycle 8051 core. Adopting a unique low-power design technology and with a wide operating voltage of 2.5 ~ 5.5 V, the chip integrates 16 KB Flash, SRAM (1 KB + 256 B), 12-bit SAR ADC (1 Msps), as well as universal peripheral communication interfaces such as UART, SPI, I2C, PWM and so on.

With built-in high-speed ROSC, LDO and POR, and no crystal/LDO/reset circuit required for the board-level system, UM8004 is featured by high integration of resources, high interference immunity, high reliability, low power consumption and minimal peripheral components. It also supports Keil MDK, C language and assembly language for software development.

Applications:

- Industrial IoT terminals
- Smart city, smart home, etc.
- Intelligent sensor terminal applications
- Operator identification

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2 Functional Block Diagram

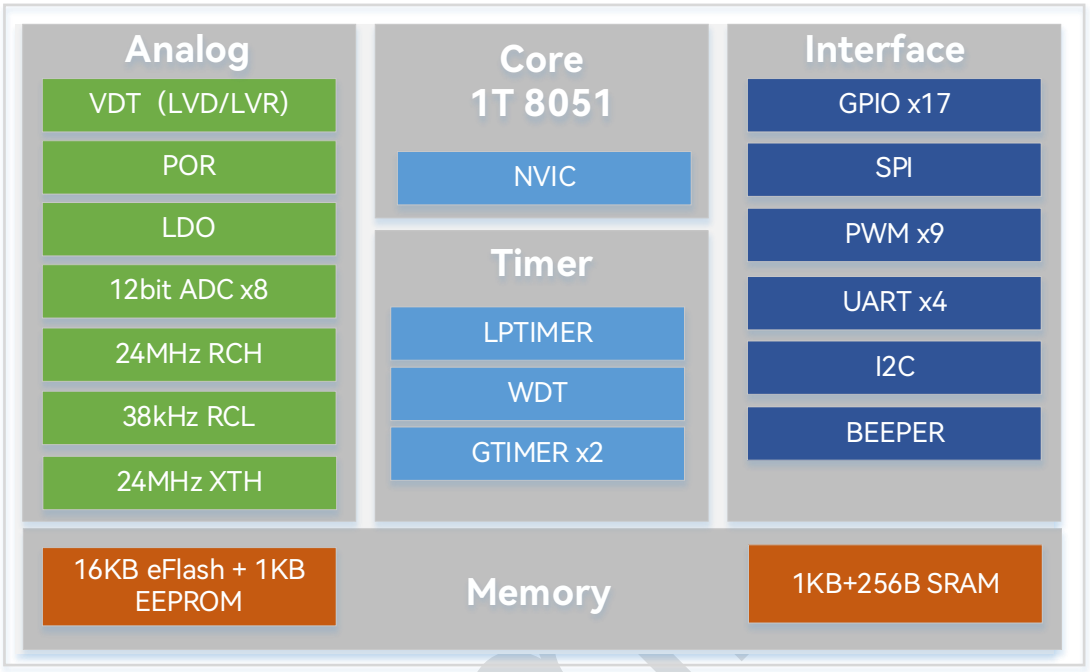


Figure 2-1: Functional Block Diagram

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3 Package and Pin Description

3.1 Pin Diagram

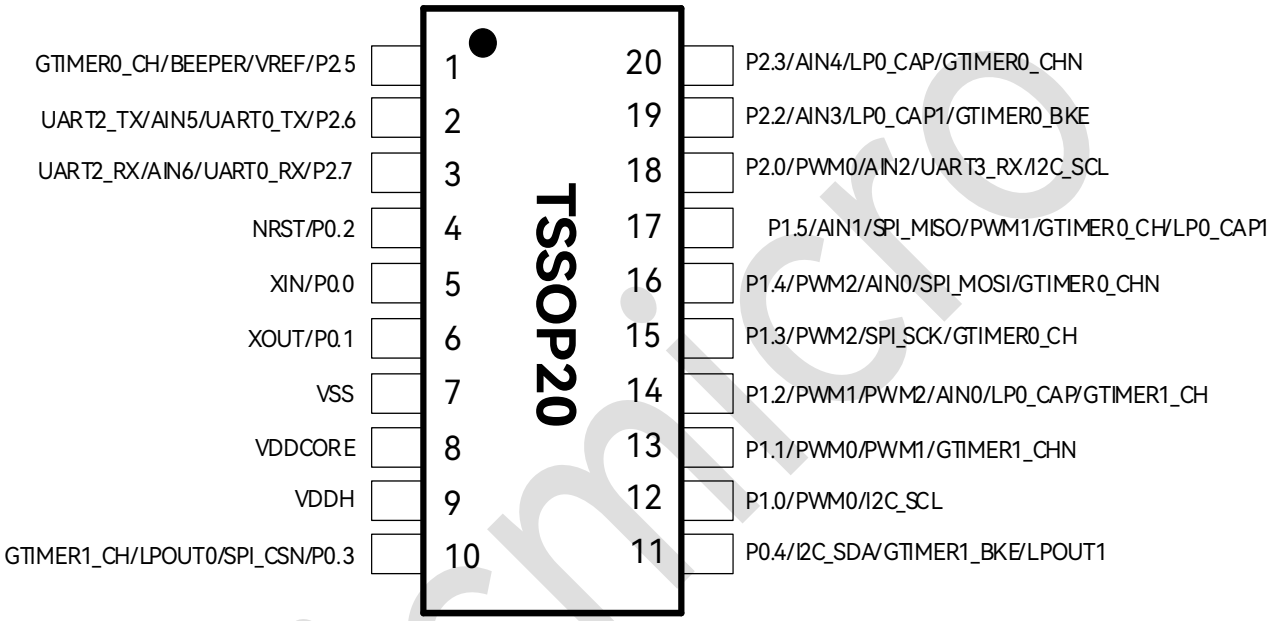


Figure 3-1: TSSOP20 Pinout Diagram

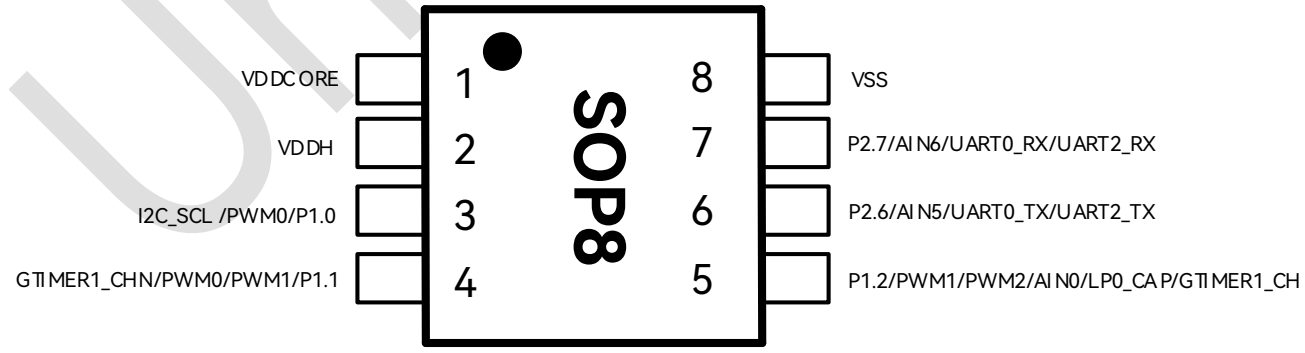


Figure 3-2: SOP8 Pinout Diagram

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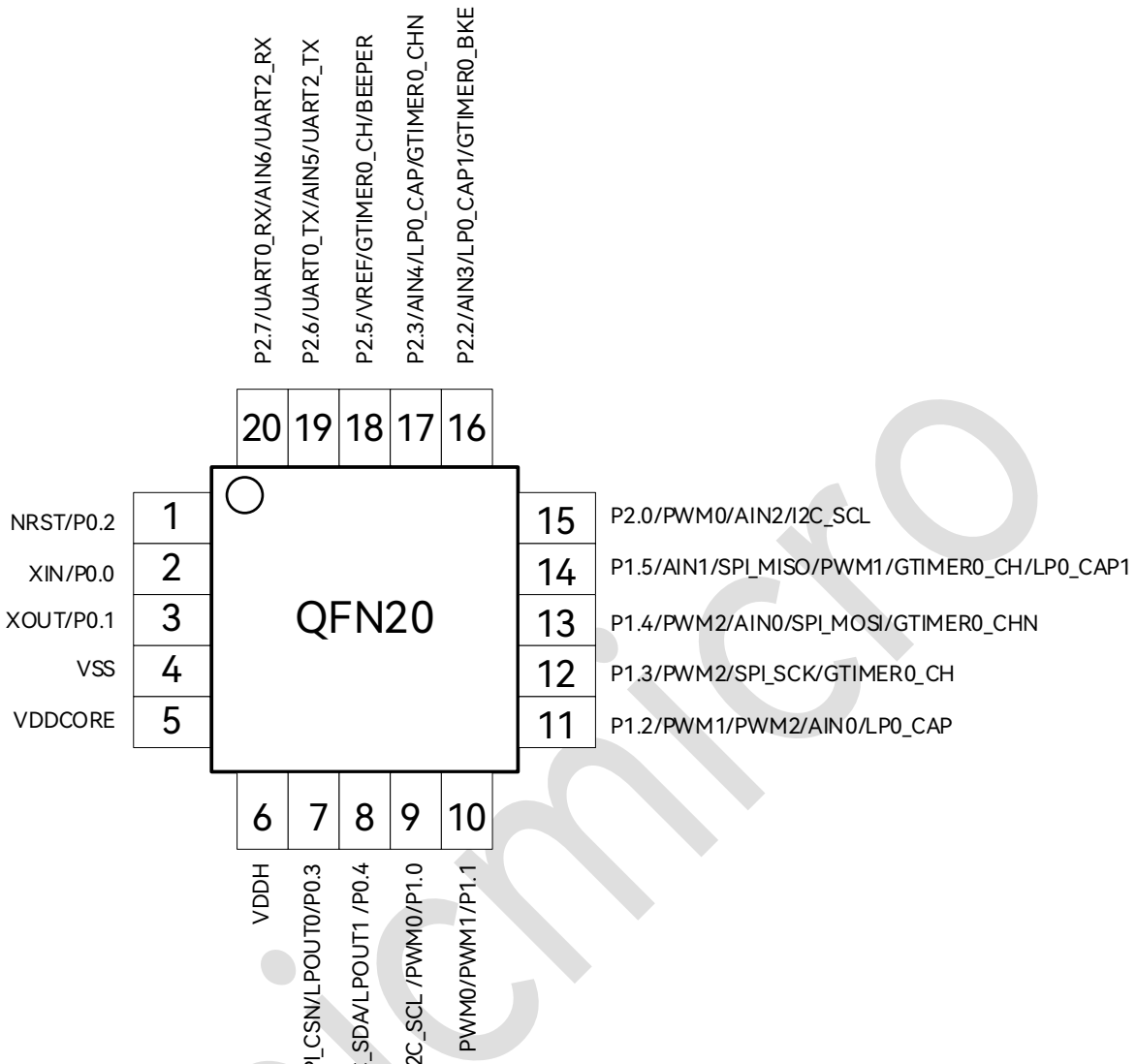


Figure 3-3: QFN20 Pinout Diagram

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3.2 Alternate Function

Table 3-1: Pin Alternate Function

Pin No. in Each Package			Config	Pxx_CFG[2:0]							
TSSOP20	SOP8	QFN20		0	1	2	3	4	5	6	7
1	-	18	V_{REF}	P2.5	UART3_TX	SPI_CSN	I2C_SCL	GTIMER0_CH	GTIMER0_BKE	BEEPER	UART0_RX
2	6	19	AIN5	P2.6	UART0_TX	UART2_TX	SPI_MISO	LPOUT1	GTIMER1_CH	-	-
3	7	20	AIN6	P2.7	UART0_RX	UART2_RX	SPI_MOSI	I2C_SCL	GTIMER1_CHN	-	BEEPER
4	-	1	NRST/P0.2	-	-	-	-	-	-	-	-
5	-	2	XIN	P0.0	UART2_RX	SPI_CSN	LPOUT0	GTIMER1_CHN	-	-	-
6	-	3	XOUT	P0.1	UART2_TX	SPI_SCK	I2C_SDA	LPOUT1	GTIMER0_BKE	-	-
7	8	4	VSS	-	-	-	-	-	-	-	-
8	1	5	VDDCORE	-	-	-	-	-	-	-	-
9	2	6	V_{DDH}	-	-	-	-	-	-	-	-
10	-	7	LPT_OUT	P0.3	CLKOUT	UART2_TX	UART3_RX	SPI_CSN	LPOUT0	GTIMER1_CH	-
11	-	8	-	P0.4	UART2_RX	SPI_SCK	I2C_SDA	LPOUT1	GTIMER1_BKE	-	-
12	3	9	-	P1.0	UART1_RX	UART2_TX	PWM0	I2C_SCL	LP0_IN	-	-
13	4	10	-	P1.1	UART1_TX	UART3_RX	PWM1	SPI_MISO	LP0_TRG	GTIMER1_CHN	PWM0
14	5	11	AIN0	P1.2	UART0_RX	UART3_TX	PWM2	LP0_CAP	GTIMER1_CH	PWM1	-
15	-	12	-	P1.3	UART0_TX	UART2_RX	SPI_SCK	I2C_SDA	LP0_IN	GTIMER0_CH	PWM2
16	-	13	AIN0	P1.4	UART1_RX	PWM2	SPI_MOSI	LP0_TRG	GTIMER0_CHN	GTIMER1_BKE	-
17	-	14	AIN1	P1.5	UART1_TX	PWM1	SPI_MISO	GTIMER0_CH	GTIMER1_BKE	-	LP0_CAP1
18	-	15	AIN2	P2.0	UART3_RX	PWM0	SPI_MOSI	I2C_SCL	LPOUT0	GTIMER0_CHN	-
19	-	16	AIN3	P2.2	UART3_TX	SPI_CSN	SPI_MISO	I2C_SDA	GTIMER0_BKE	-	LP0_CAP1
20	-	17	AIN4	P2.3	UART3_RX	SPI_SCK	SPI_MOSI	LP0_CAP	GTIMER0_CHN	-	-

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3.3 Pin Description

Table 3-2: Pin Description

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	SOP8	QFN20			DIR	PU PD		
1	-	18	P2.5	I/O	DI	-	P2.5 (default)	General-purpose digital input/output pin
							BEEPER	Buzzer output signal
							V_{REF}	V_{REF} input of ADC
							UART0_RX	RX signal of UART0
							UART3_TX	TX signal of UART3
							SPI_CSN	CS signal of SPI
							I2C_SCL	SCL signal of I2C
							GTIMER0_CH	Capture and PWM signals of GTimer0
							GTIMER0_BKE	Braking signal of GTimer0
2	6	19	P2.6	I/O	DI	-	P2.6 (default)	General-purpose digital input/output pin
							UART0_TX	TX signal of UART0
							AIN5	CH5 signal of ADC
							UART2_TX	TX signal of UART2 (for download via BOOT UART, and shall be used with NRST signal.)
							SPI_MISO	MISO signal of SPI
							LPOUT1	PWM1 signal of LPTimer
							GTIMER1_CH	Capture and PWM signals of GTimer1
3	7	20	P2.7	I/O	DI	-	P2.7 (default)	General-purpose digital input/output pin
							UART0_RX	RX signal of UART0
							AIN6	CH6 signal of ADC

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Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	SOP8	QFN20			DIR	PU PD		
							UART2_RX	RX signal of UART2 (for download via BOOT UART and shall be used with NRST signal.)
							SPI_MOSI	MOSI signal of SPI
							I2C_SCL	SCL signal of I2C
							GTIMER1_CHN	PWM reverse signal of GTimer1
							BEEPER	Buzzer signal
4	-	1	P0.2	I/O	DI	PU	NRST (default)	Reset pin for low-level reset and internal forced pull-up. This signal is necessary for batch download via UART, it is recommended to access this pin signal (pad or pin) onto PCB.
							P0.2	General-purpose digital input/output pin
5	-	2	P0.0	I/O	DI	-	P0.0 (default)	General-purpose digital input/output pin
							XIN	Crystal oscillator input pin
							UART2_RX	RX signal of UART2
							SPI_CSN	CS signal of SPI
							LPOUT0	PWM0 signal of LPTimer
							GTIMER1_CHN	PWM reverse signal of GTimer1
6	-	3	P0.1	I/O	DI	-	P0.1 (default)	General-purpose digital input/output pin
							XOUT	Crystal oscillator output pin
							UART2_TX	TX signal of UART2
							SPI_SCK	SCK signal SPI

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Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	SOP8	QFN20			DIR	PU PD		
							I2C_SDA	SDA signal of I2C
							LPOUT1	PWM1 signal of LPTimer
							GTIMER0_BKE	Braking signal of GTimer
7	8	4	VSS	G	AP	-	VSS	Connect to PCB ground
8	1	5	VDDCORE	P	AP	-	VDDCORE	2.5-V output of internal LDO (1-μF capacitance is required)
9	2	6	V_{DDH}	P	AP	-	V_{DDH}	Chip supply 2.5–5.5 V
10	-	7	P0.3	I/O	DI	-	P0.3 (default)	General-purpose digital input/output pin
							LPT_OUT	Output signal of LPTimer
							CLKOUT	Output signal of clock
							UART2_TX	TX signal of UART2
							UART3_RX	RX signal of UART3
							SPI_CSN	CS signal of SPI
							LPOUT0	PWM0 signal of LPTimer
							GTIMER1_CH	Capture and PWM signals of GTimer1
11	-	8	P0.4	I/O	DI	-	P0.4 (default)	General-purpose digital input/output pin
							UART2_RX	RX signal of UART2
							SPI_SCK	SCK signal SPI
							I2C_SDA	SDA signal of I2C
							LPOUT1	PWM1 signal of LPTimer
							GTIMER1_BKE	Braking signal of GTimer1
12	3	9	P1.0	I/O	DI	-	P1.0 (default)	General-purpose digital input/output pin
							PWM0	PWM0 signal
							LP0_IN	LPTimer input signal
							I2C_SCL	SCL signal of I2C

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Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	SOP8	QFN20			DIR	PU PD		
							UART1_RX	RX signal of UART1
							UART2_TX	TX signal of UART2
13	4	10	P1.1	I/O	DI	-	P1.1 (default)	General-purpose digital input/output pin
							PWM0	PWM0 signal
							PWM1	PWM1 signal
							UART1_TX	TX signal of UART1
							UART3_RX	RX signal of UART3
							SPI_MISO	MISO signal of SPI
							LP0_TRG	Trigger signal of LPTimer0
							GTIMER1_CHN	PWM reverse signal of GTimer1
14	5	11	P1.2	I/O	DI	-	P1.2 (default)	General-purpose digital input/output pin
							PWM2	PWM2 signal
							AIN0	CH0 signal of ADC
							PWM1	PWM1 signal
							UART0_RX	RX signal of UART0
							UART3_TX	TX signal of UART3
							LP0_CAP	Capture signal of LPTimer0
							GTIMER1_CH	Capture and PWM signals of GTimer1
15	-	12	P1.3	I/O	DI	-	P1.3 (default)	General-purpose digital input/output pin
							UART0_TX	TX signal of UART0
							PWM2	PWM2 signal
							UART2_RX	RX signal of UART2
							SPI_SCK	SCK signal SPI
							I2C_SDA	SDA signal of I2C
							LP0_IN	LPTimer input signal
							GTIMER0_CH	Capture and PWM signals of GTimer0

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Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	SOP8	QFN20			DIR	PU PD		
16	-	13	P1.4	I/O	DI	-	P1.4 (default)	General-purpose digital input/output pin
							UART1_RX	RX signal of UART1
							AIN0	CH0 signal of ADC
							SPI_MOSI	MOSI signal of SPI
							PWM2	PWM2 signal
							LP0_TRG	Trigger signal of LPTimer0
							GTIMER0_CHN	PWM reverse signal of GTimer0
							GTIMER1_BKE	Braking signal of GTimer1
17	-	14	P1.5	I/O	DI	-	P1.5 (default)	General-purpose digital input/output pin
							UART1_TX	TX signal of UART1
							SPI_MISO	MISO signal of SPI
							AIN1	CH1 signal of ADC
							PWM1	PWM1 signal
							GTIMER0_CH	Capture and PWM signals of GTimer0
							GTIMER1_BKE	Braking signal of GTimer1
							LP0_CAP1	Capture1 signal of LPTimer
18	-	15	P2.0	I/O	DI	-	P2.0 (default)	General-purpose digital input/output pin
							AIN2	CH2 signal of ADC
							UART3_RX	RX signal of UART3
							PWM0	PWM0 signal
							SPI_MOSI	MOSI signal of SPI
							I2C_SCL	I2C_SCL
							LPOUT0	PWM0 signal of LPTimer
							GTIMER0_CHN	PWM reverse signal of GTimer0

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Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	SOP8	QFN20			DIR	PU PD		
19	-	16	P2.2	I/O	DI	-	P2.2 (default)	General-purpose digital input/output pin
							AIN3	CH3 signal of ADC
							UART3_TX	TX signal of UART3
							SPI_CSN	CS signal of SPI
							SPI_MISO	MISO signal of SPI
							I2C_SDA	SDA signal of I2C
							GTIMER0_BKE	Braking signal of GTimer0
							LP0_CAP1	Capture1 signal of LPTimer
20	-	17	P2.3	I/O	DI	-	P2.3 (default)	General-purpose digital input/output pin
							AIN4	CH4 signal of ADC
							UART3_RX	RX signal of UART3
							SPI_SCK	SCK signal SPI
							SPI_MOSI	MOSI signal of SPI
							LP0_CAP	Capture signal of LPTimer0
							GTIMER0_CHN	PWM reverse signal of GTimer0

Notes:

A—analog signal; D—digital signal; I—input; O—output; G—ground; P—power; PU—pull-up; PD—pull-down; HZ—high impedance state.

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4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1: Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
V_{SS}	External supply voltage	-0.3	-	V
V_{DDH}*		-	+6.0	V
T_{stg}	Storage temperature	-55	+150	℃
T_J	Junction temperature	-40	+125	℃
I_{DD}	Max. input current of V_{DDH} pin	-	50	mA
I_{SS}	Max. output current of V_{SS} pin	-	50	mA
$V_{ESD(HBM)}$	ESD protection voltage	-8	+8	kV

Note:*: The input voltage of IO pin shall not exceed V_{DDH}, otherwise the chip will be damaged.

4.2 Operating Condition

4.2.1 General Operating Condition

Table 4-2: General Operating Condition

Symbol	Description		Min.	Max.	Unit
V_{DDH}	Operating voltage		2.5	5.5	V
T_A	Ambient temperature	f_{sys} = 24 MHz	-40	+85	℃
		f_{sys} ≤ 16 MHz	-40	+105	℃
f_{sys}	System frequency		0.1*	24	MHz

Note*: When f_{sys} is lower than 2 MHz, Flash can only fetch and execute code, but cannot erase or write.

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4.2.2 Operating Condition at Power-up / Power-down

Table 4-3: Operating Condition at Power-up / Power-down

Symbol	Description	Min.	Max.	Unit
t_{VCC}	VCC rise time rate	0	110000	μs/V
	VCC fall time rate	0	110000	

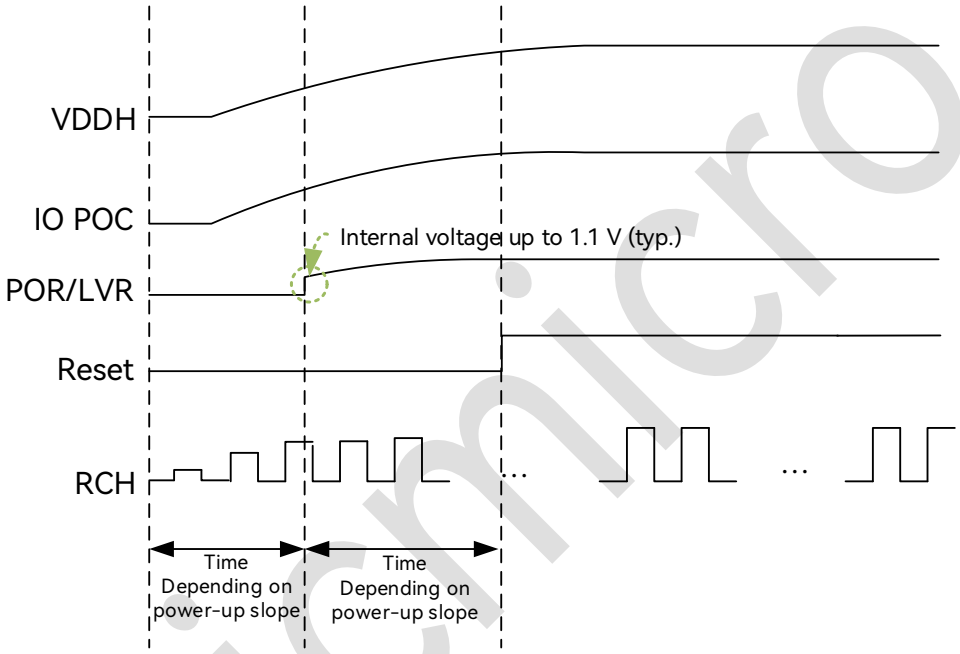


Figure 4-1: Power-on Sequence Diagram

Note: In the case of low-voltage reset occurs during power-down, the whole power-up process shall be experienced after powering up again.

4.2.3 VDT Voltage Detection (LVR/LVD)

Unless otherwise specified, V_{DDH} = 3.3 V, T_A = -40 ~ 105℃.

Table 4-4: Low Voltage Detection (LVR) Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IN_LVR}	Input detection voltage range	-	0	-	V_{DD}	V
V_{LVR}	Detection threshold	Deep sleep mode	-	0.9	-	V
		Active mode	-	1.1	-	V
V_{HYS}	Hysteresis voltage	-	-	100	-	mV

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Table 4-5: Low Voltage Detection (LVD) Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IN_LVD}	Input detection voltage range	-	0	-	V_{DD}	V
V_{LVD}	Detection threshold	ADJ_LVD<3:1>=000 ADJ_LVD<3:1> =001 ADJ_LVD<3:1>=010 ADJ_LVD<3:1>=011 ADJ_LVD<3:1>=100 ADJ_LVD<3:1>=101 ADJ_LVD<3:1>=110 ADJ_LVD<3:1>=111	-	4.39 3.95 3.59 3.29 3.04 2.82 2.63 2.46	-	V
V_{HYS}	Hysteresis voltage	-	-	100	-	mV
I_{VDD}	Current consumption	-	-	800	-	nA

4.2.4 Operating Current Characteristics

Current consumption is a comprehensive indicator of various parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, flip speed of I/O pin, location of program in memory, code executed, etc.

Table 4-6: Operating Current Characteristics

Symbol	Description	Test Condition		Min.	Typ.	Max.	Unit
I_{DD}	Operating current	Active mode: V_{DDH} = 3.3 V, T_A = 25 ℃; all peripherals are disabled, the code runs “while(1){}” in Flash. CCLK = 16 MHz		-	1.28	-	mA
		Active mode: V_{DDH} = 3.3 V/5 V, T_A = 25 ℃; all peripherals are enabled, the code runs “while(1){}” in Flash.	CCLK = 16 MHz	-	1.5	-	mA
			CCLK = 4 MHz	-	0.5	-	mA
			CCLK = 2 MHz	-	0.3	-	mA
		Sleep mode: V_{DDH} = 3.3 V, T_A = 25 ℃		-	0.24	-	mA
		DeepSleep mode: V_{DDH} = 3.3 V; T_A = 25℃		-	1.1	-	μA
		Stop mode: V_{DDH} = 3.3 V; T_A = 25℃		-	0.75	-	μA

Note [1]: The typical value range is not guaranteed. The values in the list are obtained at normal voltage and room temperature.

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4.2.5 Wakeup Time from Low-power Mode

Table 4-7: Wakeup Time from Low-power Mode

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
t_{wakeup}	Time for DeepSleep mode switching to Active mode	Regulator voltage = 2.5 V, T_A = 25℃, 16MHz	-	16.6	-	μs

4.2.6 Internal Clock Source Characteristics

- **Internal RCH oscillator**

Unless otherwise specified, V_{DDH} = 3.3 V, T_A = -40~105℃.

Table 4-8: RCH Oscillator Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{HSI}	Clock frequency	T_A = -40℃ ~ 105℃	24 * (1 - 2.5%)	24	24 * (1 + 2.5%)	MHz
Duty	Duty cycle	F_{HSI} = 24 MHz	45	50	55	%
t_{SU}	Clock settling time	-	-	1.2	-	μs
I_{VDD}	Current consumption	-	-	80	-	μA

- **Internal RCL oscillator**

Unless otherwise specified, V_{DDH} = 3.3 V, T_A = -40 ~ 105℃.

Table 4-9: RCL Oscillator Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{LSI}	Clock frequency	After trimming	38 * (1 - 5%)	38	38 * (1 + 5%)	kHz
Duty	Duty cycle	-	48	50	52	%
t_{SU}	Clock settling time	-	-	100	200	μs
I_{VDD}	Current consumption	-	-	260	-	nA

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4.2.7 External Crystal Oscillator XTH Characteristics

Unless otherwise specified, V_{DDH} = 3.3 V, T_A = -40 ~ 105℃.

Table 4-10: XTH Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Frequency range	-	2.0	16	24	MHz
t_{SU}	Clock settling time	-	-	2	-	ms
I_{VDD}	Current consumption	-	-	0.9	-	mA
I_{lk}	Leakage current	-	-	0.01	-	μA

4.2.8 Memory Characteristics

Table 4-11: eFlash Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
ECflash	Sector endurance	-	20 K	-	-	cycle
RETflash	Data retention	-	10	-	-	years
t_{prog}	Word program time	-	-	-	20	μs
t_{erase}	Sector erase time	-	2	-	5	ms
	Chip erase time	-	20	-	40	ms

4.2.9 IO Characteristics

Table 4-12: IO Characteristics

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{IL}	Logic low level input current	V_I = 0 V	-1	-	-	μA
I_{IH}	Logic high level input current	$V_I = V_{DDH}$	-	-	+1	μA
V_O	Output voltage	Output pin being active	0	-	V_{DD}	V
V_{IH}	Logic high level input voltage	-	0.7 * V_{DDH}	-	-	V
V_{IL}	Logic low level input voltage	-	-	-	0.3 * V_{DDH}	V
V_{hys}	Hysteresis voltage	-	0.1 * V_{DDH}	-	-	V

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Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
V_{OH}	Logic high level output voltage	5 V, normal output of I_{Load} = 16 mA in high-drive mode and I_{Load} = 8 mA in low-drive mode.	V_{DDH} - 0.8	-	-	V
		3.3 V, normal output of I_{Load} = 8 mA in high-drive mode and I_{Load} = 4 mA in low-drive mode.	2.4	-	-	V
V_{OL}	Logic low level output voltage	5 V, normal output of I_{Load} = 16 mA in high-drive mode and I_{Load} = 8 mA in low-drive mode.	-	-	0.5	V
		3.3 V, normal output of I_{Load} = 8 mA in high-drive mode and I_{Load} = 4 mA in low-drive mode.	-	-	0.4	V
I_{OH}	Logic high level output current	5 V, output in high-drive mode output in low-drive mode	- -	16 8	- -	mA
		3.3 V, output in high-drive mode output in low-drive mode	- -	8 4	- -	mA
I_{OL}	Logic low level output current	5 V, output in high-drive mode output in low-drive mode	- -	16 8	- -	mA
		3.3 V, output in high-drive mode output in low-drive mode	- -	8 4	- -	mA
R_{pup} R_{pdn}	Pull up / down current	5 V / 3.3 V	20	-	100	kohm
CIN	Input capacitance	5 V / 3.3 V	-	-	10	pF

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4.2.10 ESD/Latchup Characteristics

All the data below are measured at T_A = +25℃ based on ESDA/JEDEC standard.

Table 4-13: ESD/Latchup Characteristics

Symbol	Description	Class	Max.	Unit
$V_{ESD(HBM)}$	ESD @ Human Body Model	Class 3B	8000	V
$V_{ESD(CDM)}$	ESD @ Charge Device Model	Class C2	500	V
$V_{ESD(MM)}$	ESD @ Machine Model	Class B	200	V
$I_{latchup}$	Latch up current	Class IA	200	mA

4.2.11 ADC Characteristics

The following electrical characteristics are measured at T_A= 25℃, V_{DDH}= 3.3 V and V_{DDD25} = 2.5 V.

Table 4-14: ADC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{ADCIN}	Input voltage range	Single ended	0	-	V_{DDH}	V
V_{REF}	ADC reference voltage	-	-	V_{DDH}	-	V
I_{ADC}	-	-	0.7	0.9	1.2	mA
C_{ADCIN}	ADC input capacitance	-	3.5	4	4.5	pF
f_{ADCCLK}	ADC clock frequency	-	0.5	4	16	MHz
$t_{ADCSTART}$	Startup time of ADC bias current	-	2	3	4	μs
$t_{ADCCONV}$	Conversion time	-	16	16	20	cycle
ENOB	-	-	9.5	10	10.4	bit
DNL	Differential non-linearity	-	-2	±1	2	LSB
INL	Integral non-linearity	-	-3	±1	3	LSB
E_o	Offset error	-	-2	±1	2	LSB
E_g	Gain error	-	-2	±1	2	LSB

Note: Not tested in production.

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4.3 Power Supply Scheme

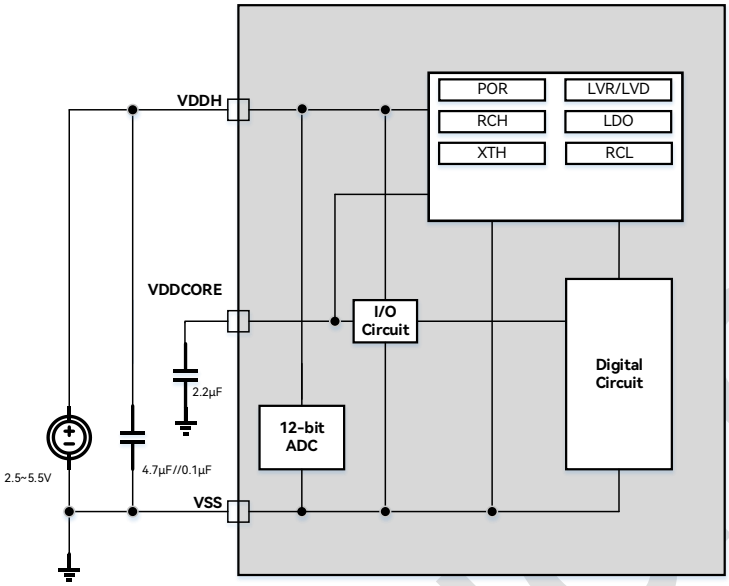


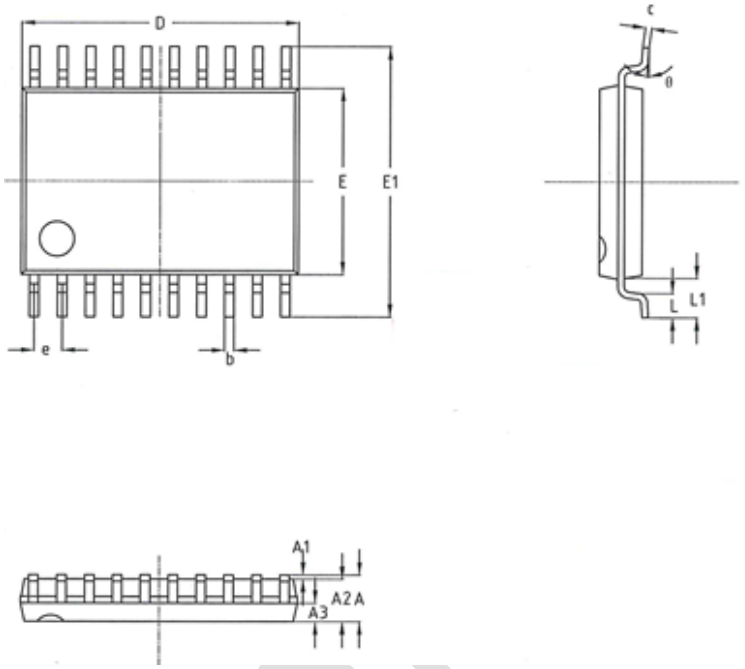
Figure 4-2: Power Supply Schematic diagram

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5 Package Outline

5.1 TSSOP20 (6.5 * 4.4 mm)

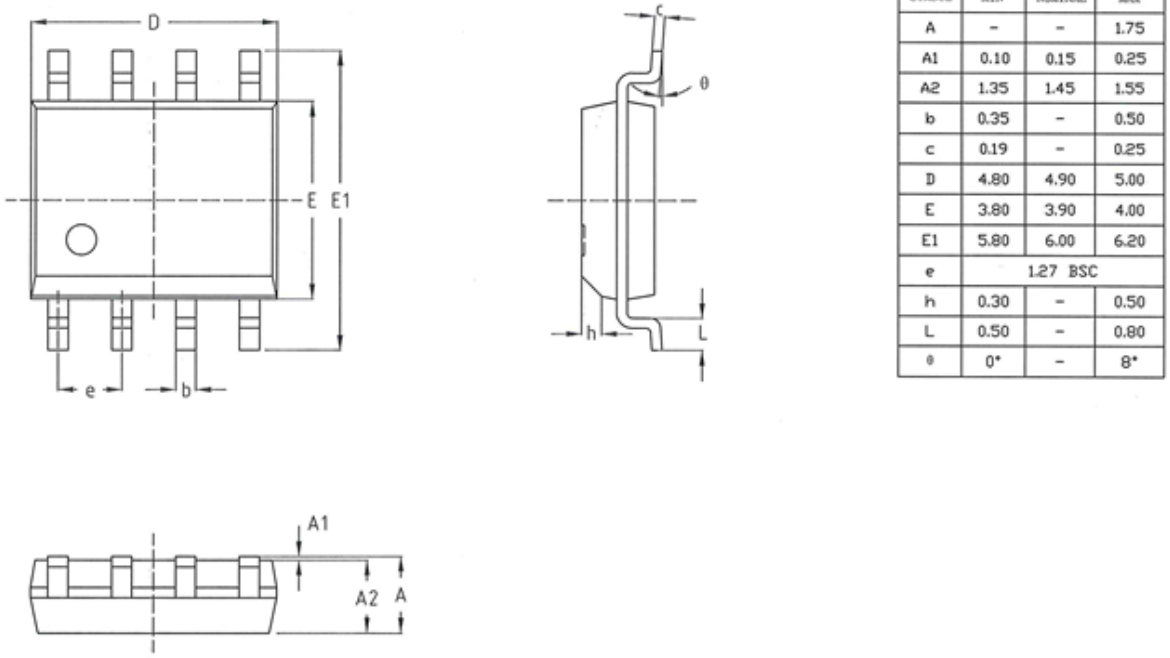


Dimensions/mm			
SYMBOL	MIN	NOMINAL	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
c	0.13	-	0.17
D	6.40	6.50	6.60
E	4.30	4.40	4.50
E1	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00REF		
L	0.45	0.60	0.75
θ	0°	-	8°

Figure 5-1: TSSOP20 Package Outline

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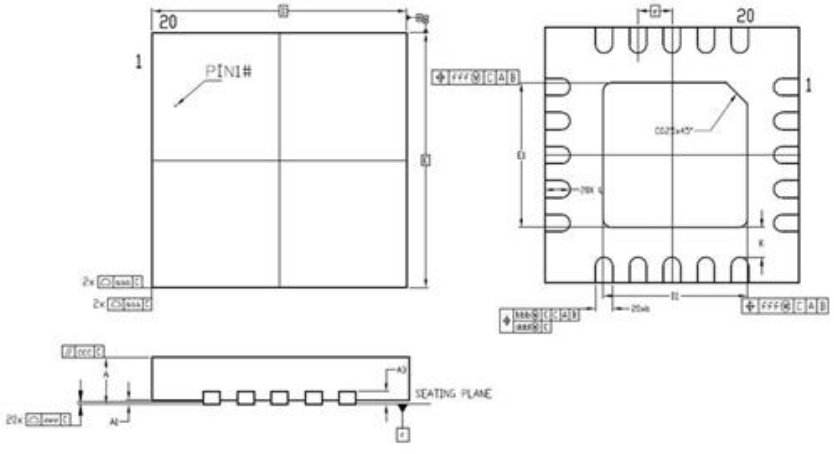
5.2 SOP8 (4.9 * 3.9 mm)



Dimensions/mm			
SYMBOL	MIN	NOMINAL	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.35	1.45	1.55
b	0.35	-	0.50
c	0.19	-	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.30	-	0.50
L	0.50	-	0.80
θ	0°	-	8°

Figure 5-2: SOP8 Package Outline

5.3 QFN20 (3 * 3 mm)



DIM / SYMBOL	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3	-	0.152 REF	-
b	0.15	0.20	0.25
D	3.00BSC		
E	3.00BSC		
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e	0.40BSC		
L	0.20	0.30	0.40
K	0.20	-	-
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 5-3: QFN20 Package Outline

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6 Revision History

Version	Date	Modifications
V1.0	Jan-13-2022	Initial release.
V1.1	Feb-10-2022	1. Updated QFN20 package outline drawing. 2. Updated pin descriptions. 3. Updated TSSOP20 package outline drawing. 4. Updated DC parameters. 5. Deleted descriptions regarding T0/T1. 6. Updated parameters regarding the internal RCL oscillator.
V1.2	Mar-11-2022	1. Added information on the 1-KB EEPROM in the chapter of Features. 2. Updated the pinout diagrams. 3. Added the chapter of Pin Configuration. 4. Updated pin descriptions. 5. Updated parameters regarding the internal RCH oscillator.
V1.3	Mar-28-2022	1. Added “4.2.2 Operating Condition at Power-up / Power-down” chapter. 2. Updated parameters regarding the internal RCH oscillator. 3. Updated the range of operating temperature.
V1.4	Apr-22-2022	1. Updated the SOP8 package outline drawing. 2. Updated the value of 1.5 V into 2.5 V in the whole document. 3. Updated the chapter of Pin Configuration. 4. Updated the bit 7 description of P13_CFG[2:0] into PWM2.
V1.5	Jul-13-2022	Adjusted the structures of the chapter Features and the chapter Electrical Specifications.
V1.5.1	Jun-24-2024	1. Updated the notes regarding UART0 and UART2 of pins P2.6 and P2.7 in the chapter of Pin Description. 2. Updated the tolerance of L from 0.3±0.05 to 0.3±0.1 in QFN20 package outline. 3. Deleted the original chapter of 4.2.10 Port Characteristics. 4. Replaced the font and updated the formatting.
V1.5.2	Aug-26-2024	Updated the typical values of V_{LVD} in “Table 4-5: Low Voltage Detection (LVD) Characteristics”.
V1.5.3	May-12-2025	Added “4.3 Power Supply Scheme” chapter.

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